QSOLID

www.q-solid.de

Quantum Computer in the Solid State

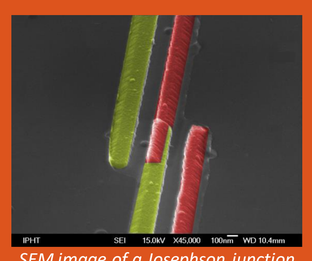
Technology development and realization of superconducting hardware for quantum-computer demonstrator

Short overview

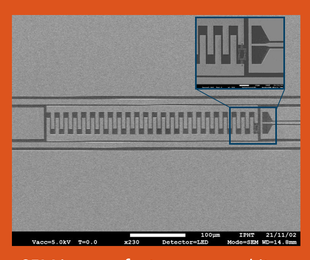
- Effective research foundry for the consortium; especially fabricate quantum processor units (QPUs) and readout amplifiers.
- Evolve existing and research novel fabrication processes for high throughput and optimized parameters concerning coherence, reproducibility, and spread.
- Develop circuits for scaling especially improving traveling wave parametric amplifiers (TWPAs) as well as digital superconducting electronics.
- Research towards new materials, optimize operational process in fabrication and optimization and bundle results into foundry service at project end.

Experience

Fabrication of superconducting circuits, including Al shadow evaporation and Nb cross-type process.



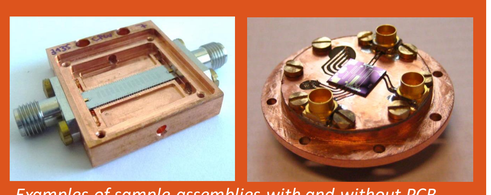
SEM image of a Josephson junction fabricated by shadow evaporation technique.



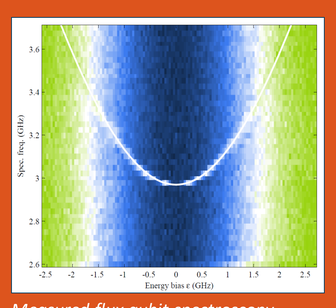
SEM image of a transmon qubit.

Simulation and design of quantum bits, mostly flux qubits but also transmons.

Assembling and interconnection technologies.
System integration for instrument implementation.



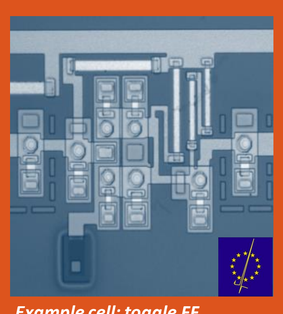
Examples of sample assemblies with and without PCB board.



Measured flux qubit spectroscopy. Transmission phase as a function of energy bias and qubit driving frequency.

Experimental investigations of qubits coupled to resonators at mK temperatures.

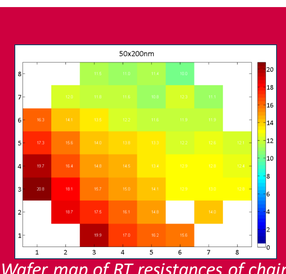
ISO certified fabrication processes for digital superconducting circuits based on rapid single flux quantum logic accessible in frame of FLUXONICS foundry.



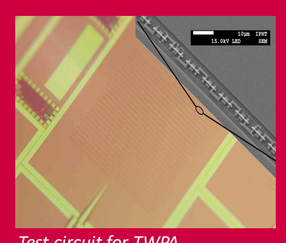
Example cell: toggle FF, www.FLUXONICS-Foundry.de

Aims and tasks

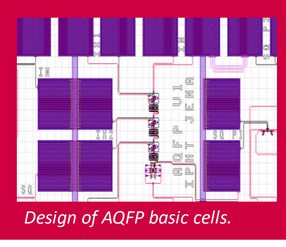
- Implement a wafer-scale fabrication of superconducting qubits with high coherence and low parameter spread,
- Develop suitable integration technologies for scalable interconnection such as through silicon vias and innovative bonding techniques,
- Fabricate qubit-circuits of small to medium size to half time QPU,
- Develop designs for high performance quantum bits,
- Simulate, design, and fabricate TWPAs to be used for in the demonstrator; experimentally determine their performance,
- Circuit development of digital superconducting electronics based on adiabatic quantum flux parametron cells in second project half,
- Transfer the R&D technologies into a research foundry and offer it to partners at the end of the project.



Wafer map of RT resistances of chains of 10 Josephson $(0.2\mu m)^2$ junctions.

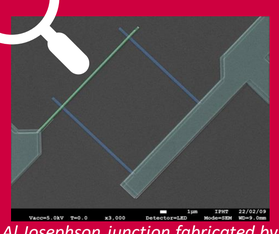


Test circuit for TWPA.

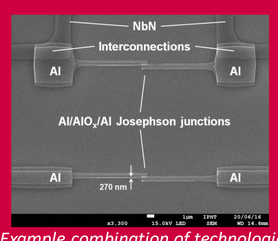


Design of AQFP basic cells.

Methods



Al Josephson junction fabricated by Manhattan technique.



Example combination of technologies.

Deposition cluster.

- Introduce Manhattan type Josephson junction fabrication and optimize for small junction sizes of about 0.1x0.1 μm^2,
- Introduce additional process steps for surface and interface control; upgrade fabrication tools and introduce new materials such as NbN,
- Implement fast measurement feedback cycles by advancing experimental equipment and automation,
- Standardize test circuits; use resonator quality as fast quality indicator,
- Make use of fabrication evaluation techniques available in consortium,
- Test and use room-temperature electronics developed in the consortium,
- Make use of characterization techniques developed by theory partners,
- Introduce quality evaluation and management methods for fabrication and experiments; create process descriptions and cell library.

Fabrication methods development

Novel materials and process steps

Continuous process monitoring

Automatized characterization

Superconducting circuit development

Cell library definition

Fabrication of key components

Process description

Quantum computer demonstrator

Research foundry

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Poster link